IN THE CLAIMS

Please amend claims 1 and 18 in accordance with the following listings showing the status of all claims in the application.

1. (Currently Amended) A method of computing delays of a cell in an integrated circuit, ~~said cell having parameters including a process, supply voltage, temperature, input ramptime and output load,~~ the method comprising the steps of:

(a) generating a first set of the delays of ~~the~~a cell by assigning nominal values to parameters of the cell, said parameters including: a process, supply voltage, temperature, input ramptime and output load;

(b) generating a second set of the delays of the cell by varying values assigned to the parameters of the cell;

(c) creating a delay equation based on the first set and second set of the delays; and

(d) computing the delays of the cell by using the delay equation,

wherein the delay equation characterizes the delays in terms of the parameters of the cell.

2. (Original) The method of claim 1, wherein step (a) comprises setting the process to a nominal process, the supply voltage to a nominal voltage and the temperature to a nominal temperature.

3. (Original) The method of claim 2, wherein step (a) further comprises varying the input ramptime and the output load during the generation of the first set of the delays.

4. (Original) The method of claim 3, wherein the input ramptime is varied from a minimum allowable input ramptime to a maximum allowable input ramptime.

5. (Original) The method of claim 4, wherein the output load is varied from a minimum allowable output load to a maximum allowable output load.

6. (Original) The method of claim 1, wherein step (b) comprises varying the process to a non-nominal process.

7. (Original) The method of claim 6, wherein step (b) further comprises varying the supply voltage to a non-nominal supply voltage.

8. (Original) The method of claim 7, wherein step (b) further comprises varying the temperature to a non-nominal temperature.

9. (Original) The method of claim 8, wherein the input ramptime is varied from a minimum allowable input ramptime to a maximum allowable input ramptime.

10. (Original) The method of claim 9, wherein the output load is varied from a minimum allowable output load to a maximum allowable output load.

11. (Original) The method of claim 1, further comprising the step of generating a set of coefficients related to the process, the supply voltage and the temperature based on the first and second set of the delays.

12. (Original) The method of claim 11, wherein step (c) comprises the step of inserting the set of coefficients into the delay equation.

13. (Original) A method of computing delays of a cell in an integrated circuit, the method comprising the steps of:

generating a first set of the delays of the cell in a first simulation by using nominal values for a process, supply voltage and temperature of the cell;

assigning a time value within a first range to an input ramptime of the cell during the generation of each of the delays in the first set;

assigning a load value within a second range to an output load of the cell during the generation of each of the delays in the first set;

generating a second set of the delays of the cell in a second simulation by using non-nominal values for the process, supply voltage and temperature of the cell;

creating a delay equation based on the first set and second set of the delays; and

computing the delays of the cell by using the delay equation,

wherein the delay equation characterizes the delays in terms of the process, supply voltage, temperature, input ramptime and output load of the cell.

14. (Original) The method of claim 13, further comprising the steps of:

assigning the time value within the first range to the input ramptime of the cell during the generation of each of the delays in the second set; and

assigning the load value within the second range to the output load of the cell during the generation of each of the delays in the second set.

15. (Original) The method of claim 14, further comprising the step of generating a set of coefficients related to the process, the supply voltage and the temperature based on the first and second set of the delays.

16. (Original) The method of claim 15, further comprising the step of inserting the set of coefficients into the delay equation.

17. (Original) An apparatus for computing delays of a cell in an integrated circuit, said apparatus comprising:

a processor for executing stored program instruction steps; and

a memory connected to the processor for storing the program instruction steps,

wherein the cell has parameters including a process, supply voltage, temperature, input ramptime and output load, and the program instruction steps include:

generating a first set of the delays of the cell by assigning nominal values to the parameters;

generating a second set of the delays of the cell by varying values assigned to the parameters of the cell;

creating a delay equation based on the first set and second set of the delays; and

computing the delays of the cell by using the delay equation,

wherein the delay equation characterizes the delays in terms of the parameters of the cell.

18. (Currently Amended) An ECAD system for computing delays of a cell in an integrated circuit, said system comprising:

means for generating a first set of the delays of the cell by assigning nominal values to parameters of the cell, said parameters including: a process, supply voltage, temperature, input ramptime and output load;

means for generating a second set of the delays of the cell by varying values assigned to the parameters of the cell;

means for creating a delay equation based on the first set and second set of the delays; and

means for computing the delays of the cell by using the delay equation,

wherein the delay equation characterizes the delays in terms of the parameters of the cell.

19. (Original) An apparatus for computing delays of a cell in an integrated circuit, said apparatus comprising:

a processor for executing stored program instruction steps; and

a memory connected to the processor for storing the program instruction steps,

wherein the program instruction steps include:

generating a first set of the delays of the cell in a first simulation by using nominal values for a process, supply voltage and temperature of the cell;

assigning a time value within a first range to an input ramptime of the cell during the generation of each of the delays in the first set;

assigning a load value within a second range to an output load of the cell during the generation of each of the delays in the first set;

generating a second set of the delays of the cell in a second simulation by using non-nominal values for the process, supply voltage and temperature of the cell;

creating a delay equation based on the first set and second set of the delays; and

computing the delays of the cell by using the delay equation,

wherein the delay equation characterizes the delays in terms of the process, supply voltage, temperature, input ramptime and output load of the cell.

20. (Original) The apparatus of claim 19, wherein the program instruction steps further include the steps of:

assigning the time value within the first range to the input ramptime of the cell during the generation of each of the delays in the second set; and

assigning the load value within the second range to the output load of the cell during the generation of each of the delays in the second set.

21. (Original) The apparatus of claim 20, wherein the program instruction steps further include the step of generating a set of coefficients related to the process, the supply voltage and the temperature based on the first and second set of the delays.

22. (Original) The apparatus of claim 21,wherein the program instruction steps further include the step of inserting the set of coefficients into the delay equation.